



LARN

Latency- and Resilience-Aware Networking

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SPP 1914: "Cyber-Physical Networking"

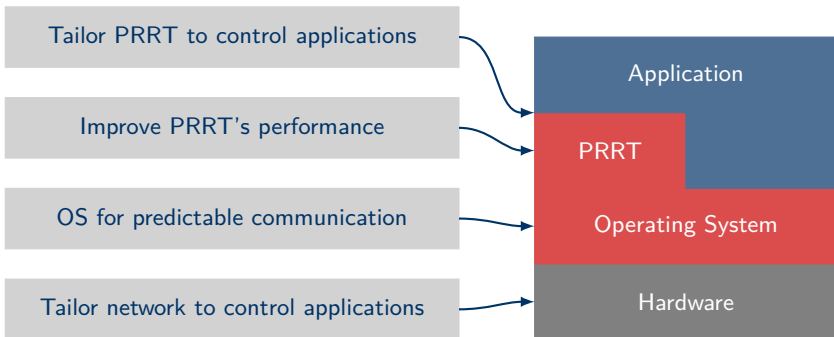
<http://larn.systems>

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November 30th, 2018

Recapitulation: Goals



Software, Hardware & Algorithms

- PRRT** Predictable Reliable Real-time Transport protocol
- Improved Packet Loss Measurement
 - Coding Configuration Optimization
 - Cross-Layer Pacing + Rate Control
 - Released stable version 0.3.1

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X-LAP Cross-Layer Timing Analysis

Δ ELTA System Modification Analysis

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X-LAP Cross-Layer Timing Analysis

Δ ELTA System Modification Analysis

RNA Reliable Networking Atom

- Drone
- Quality of Control Metrics
- Preparing release 0.9.0

Outline

Status

PRRT

X-LAP & Δ ELTA

INTspect

Conclusion

Changelog

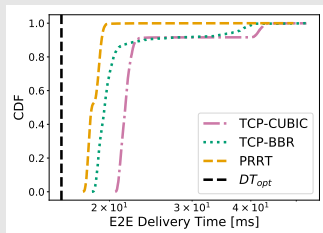
- ▶ v0.3.1 released in November
 - ▶ Congestion control inspired by BBR 1.x
 - ▶ Error control with reliable timing for ARQ
 - ▶ Improved network estimation capabilities
- ▶ v0.2.0 released in May
 - ▶ API enhancements.
 - ▶ Significant extension of the Wiki, README and other pieces of documentation.

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Components under Development

- ▶ Rate Control & Pacing:
Reduced latencies and jitter.
- ▶ Improved loss estimation
- ▶ Performance optimizations



Outline

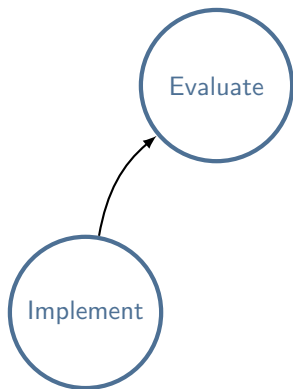
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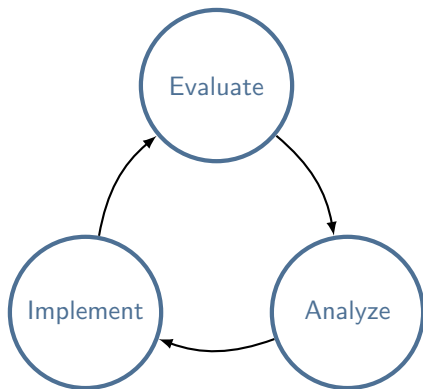
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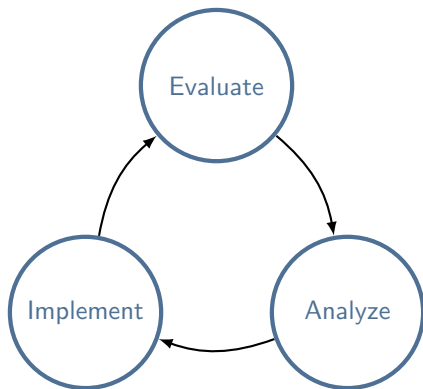
Approach:

- ▶ Measurement-based protocol evaluation



Approach:

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- ▶ Derive meaningful information
- ▶ Support protocol design

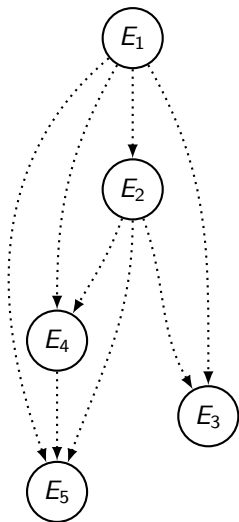


Approach:

- ▶ Measurement-based protocol evaluation
- ▶ Derive meaningful information
- ▶ Support protocol design

Challenges:

- Identify *critical code parts*
 - Latency, Jitter, Energy
- Analyze code modifications
- Automate feedback

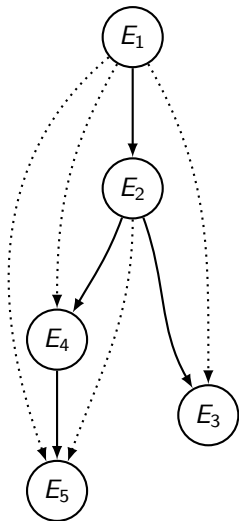


Goal:

- ▶ Reconstruct protocol information from timestamps

Control flow reconstruction:

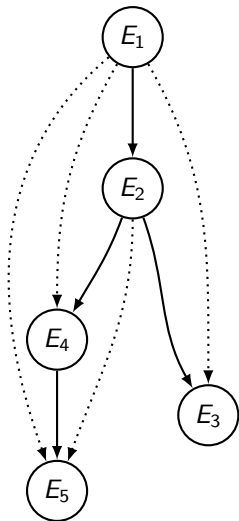
1. Compute *happens-before* relation of events

**Goal:**

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Control flow reconstruction:

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2. Compute *happens-directly-before* relation of events



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Control flow reconstruction:

1. Compute *happens-before* relation of events
2. Compute *happens-directly-before* relation of events

Edges represent:

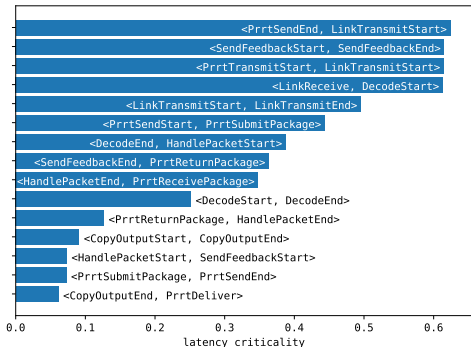
- ▶ Code segments $\langle E_i, E_j \rangle$
- ▶ Local communication
- ▶ False-positives

Goals:

- ▶ Filter out false-positive segments
- ▶ Identify code segments worth optimizing

Detect *relevant* code segments:

1. Compute the correlation between the segment latency and the E2E latency
2. Ignore segments with negative correlation



Goals:

- ▶ Filter out false-positive segments
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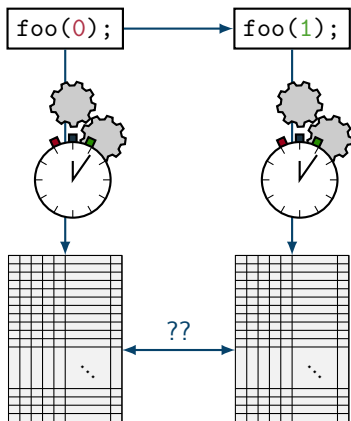
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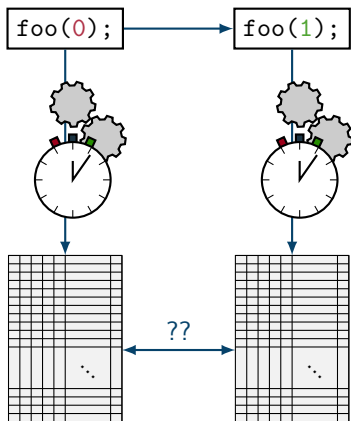
Goals:

- ▶ Evaluate the influence of code changes
- ▶ Interferences are complex



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Goals:

- ▶ Evaluate the influence of code changes
- ▶ Interferences are complex

Modification impact analysis:

1. Evaluate the original and the modified versions of the protocol
2. Apply the *k-sample Anderson-Darling-Test* on the traces
3. For each code segment, test decides: "similar" or "different"

<PrrtSendPacketStart,PrrtSendPacketEnd> has not changed
<CopyOutputStart,CopyOutputEnd> has not changed
<SendFeedbackStart,SendFeedbackEnd> has not changed
...

<PrrtSubmitPackage,PrrtSendEnd> has changed:
2.85±0.91 μ s → 4.94±0.58 μ s

<LinkReceive,DecodeStart> has changed:
2.36±3.80 μ s → 3.56±4.88 μ s
...

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Lack of Data

- ▶ Hardware complexity complicates interrupt latency predictability
- ▶ Unknown overhead for software interrupt handling mechanisms

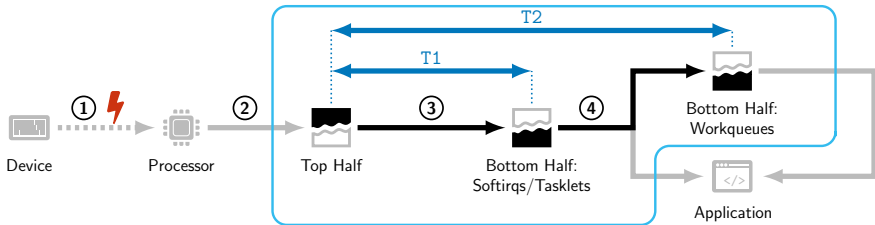
Lack of Understanding for Delay Sources

- ▶ Unknown reasons for delays
- ▶ Reasons for delays vary among interrupt handling mechanisms

Lack of Tool Support

- ▶ Tool for precise and flexible overhead measurements
- ▶ Support of different hardware architectures

Linux Interrupt Handling



Linux Interrupt Handling

- ▶ Top half
- ▶ Bottom half
 - Softirq, Tasklet, Workqueue
 - Variation in **flexibility**

INTSPECT Analysis

- ▶ Latency and Jitter analysis
- ▶ Software overhead
 - Latency **T1** and **T2**
 - Variation in **latency & jitter**

INTSPECT Architecture & Evaluation

Kernel Module

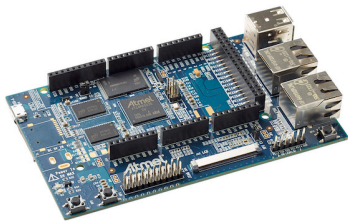
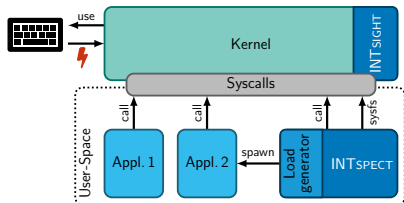
- ▶ Support all bottom half mechanisms
- ▶ Minimal run-time interference
- ▶ Portable

User-Space Component

- ▶ Analysis & Control framework
- ▶ Plugin interface
 - load generators, hardware states

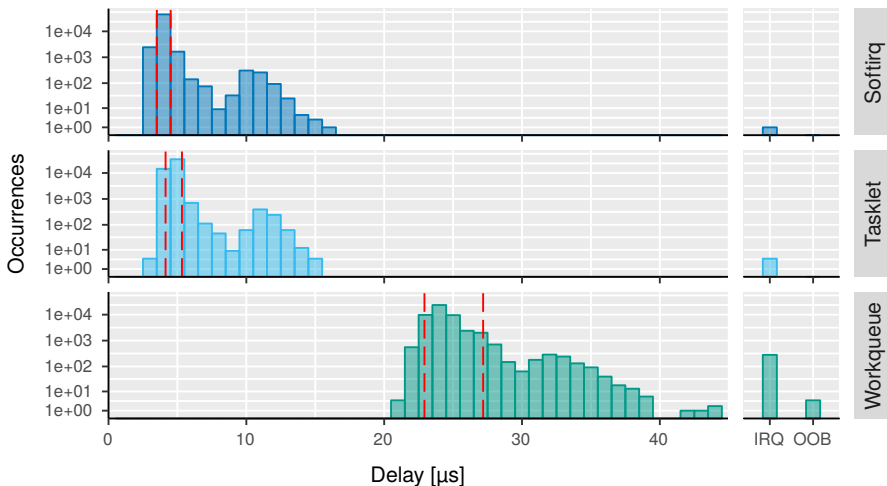
Hardware Support

- ▶ x86
- ▶ ARM → Atmel SAMA5D3 Xplained

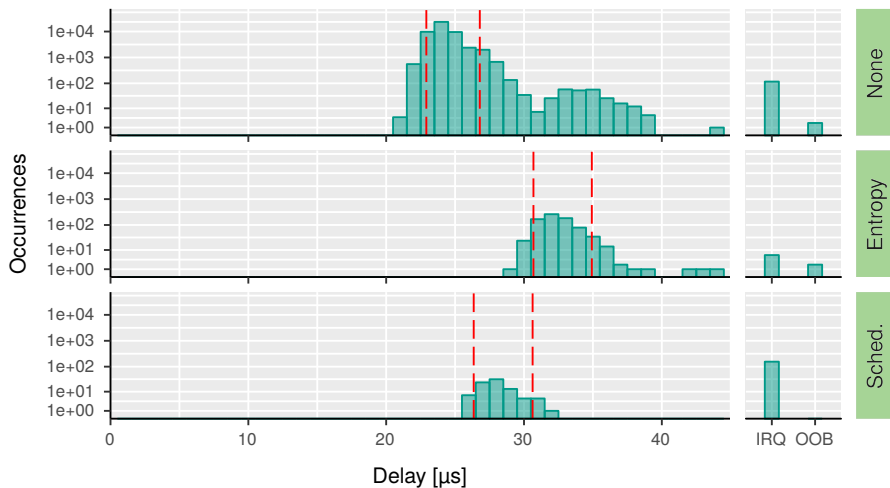




Comparison of Bottom Handler Mechanisms



Sources of Interference



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Accepted Publications

- ▶ Reif, Stefan; Schmidt, Andreas; Hönig, Timo; Herfet, Thorsten; Schröder-Preikschat, Wolfgang: “ **Δ elta: Differential Energy-Efficiency, Latency, and Timing Analysis for Real-Time Networks**”, International Workshop on Real-Time Networks (RTN), 2018
- ▶ Herzog, Benedict; Gerhorst, Luis; Heinloth, Bernhard; Reif, Stefan; Hönig, Timo; Schröder-Preikschat, Wolfgang: **INTSPECT: Interrupt Latencies in the Linux Kernel**, Brazilian Symposium on Computing Systems Engineering (SBESC), 2018.
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Publications Under Review

- ▶ Schmidt, Andreas; Reif, Stefan; Gil Pereira, Pablo; Hönig, Timo; Herfet, Thorsten; Schröder-Preikschat, Wolfgang: “**Blinded**”, Blinded, 2019.

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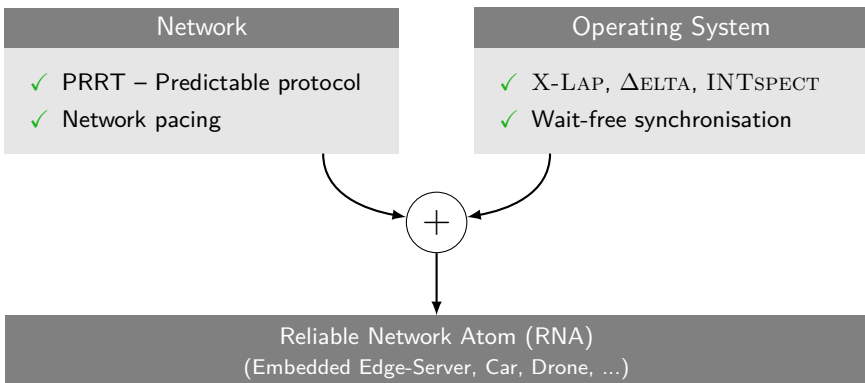
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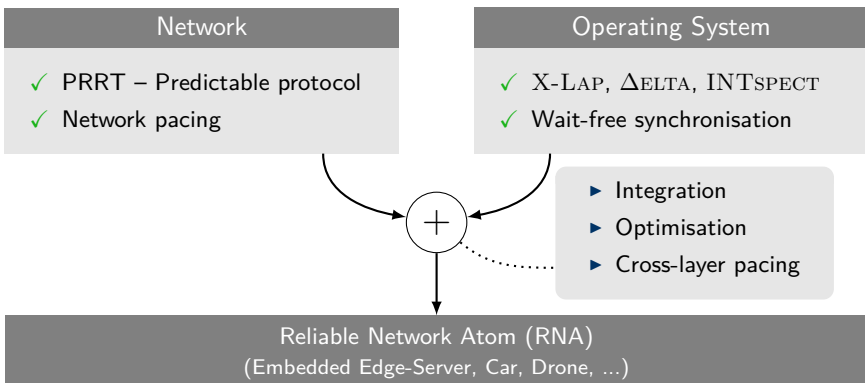
Publications in the Writing

- ▶ Joint publication based on BarCamp IV results.

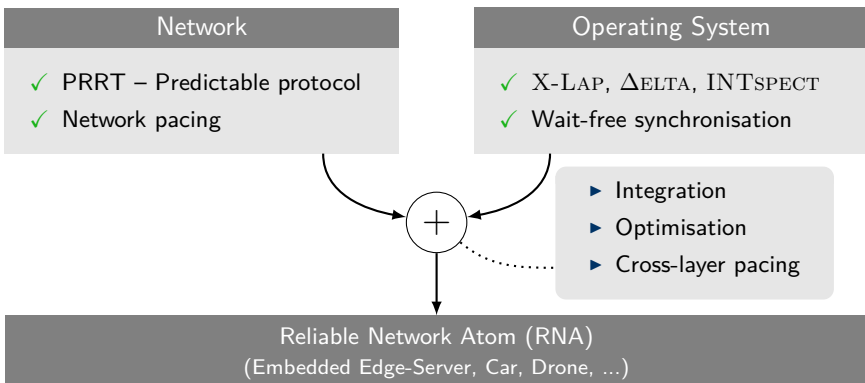
Conclusion



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Thank you for your attention. Questions?